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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,380	06/12/2006	Steven C. Deane	GB030221	5921

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS  
P.O. BOX 3001  
BRIARCLIFF MANOR, NY 10510

EXAMINER
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NHU, DAVID

ART UNIT	PAPER NUMBER
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2818

MAIL DATE	DELIVERY MODE
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08/16/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/596,380

Applicant(s)

DEANE, STEVEN C.

Examiner

David Nhu

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) 1-4 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 5-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTIONS

1. Insert –This application is a 371 of PCT/IB04/52778 filed 12/13/2004-- in the specifications.

### Specifications

#### Content of Specification

2. The following guidelines illustrate the preferred layout and content for patent applications. These guidelines are suggested for the applicant's use.

*Brief of the Invention is missing. See the arrangement of the specification below.*

#### *Arrangement of the Specification*

The following order or arrangement is preferred in framing the specification and, except for the reference to "Microfiche Appendix" and the drawings, each of the lettered items should appear in upper case, without underlining or bold type, as section headings. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) Title of the Invention.
- (b) Cross-References to Related Applications.
- (c) Statement Regarding Federally Sponsored Research or Development.
- (d) Reference to a "Microfiche Appendix" (see 37 CFR 1.96).
- (e) Background of the Invention.
  1. Field of the Invention.
  2. Description of the Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (f) Brief Summary of the Invention.
- (g) Brief Description of the Several Views of the Drawing(s).
- (h) Detailed Description of the Invention.
- (i) Claim or Claims (commencing on a separate sheet).
- (j) Abstract of the Disclosure (commencing on a separate sheet).
- (k) Drawings.

### Abstract

3. The abstract of the disclosure is objected to because legal phraseology such as "**comprise**" is used. Correction is required. See MPEP & 608.01(b).

### Claims Objection

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4. Claim 5, "the islands providing" should be --the **polycrystalline silicon** islands providing-- ;  
"the device further" should be --the **active matrix pixel** device further-- ; "the intrinsic region "  
should be --the amorphous silicon intrinsic region--

Claim 6, "the source/drain regions" should be --the **doped** source/drain regions--

Claim 8, "the islands" should be --the **polycrystalline silicon** islands-- ; "the first transistor"  
should be --a **first thin** transistor--

Claim 9, "the intrinsic region" should be --the **amorphous silicon** intrinsic region--

Claim 10, "the current" should be -- a current--; "the transistor" should be --the **thin film**  
transistor--

Claim 11, "the light intensity output" should be --a light intensity output-- ; "the light output"  
should be --the light **intensity** output--; the measured light intensity" should be --the measured  
light intensity **output**--

### ***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the  
basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public  
use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 5-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Takayama et al  
95,589,694).

**Regarding claim 5**, Takayama, (see figures 1C-1E, 9A-9C, col. 1, lines 59-67, col. 2, lines ,  
col. 18, lines 60-67, col. 19, lines 1-44), teaches an active matrix pixel device, comprising: a  
plurality of polycrystalline silicon islands 58N, 58P, 19a supported by a substrate , one of the

polycrystalline silicon islands providing a channel and doped source/drain regions 9B of a thin film transistor, the active matrix pixel further comprising a PIN diode, which includes a p-type doped region 19p, 58P and an n-type doped region 19n, 58N separated by an amorphous silicon intrinsic region 19i, 58I, wherein the amorphous silicon intrinsic region overlies and contacts at least a part of one of the polycrystalline silicon islands, which provides one of the p-type or n-type doped regions (see figures 1D, 9A).

Regarding claims 6, 7, Takayama, (see figure 9A, 9C), teaches the doped source/drain regions 9B and said one of the p-type or n-type doped regions of the PIN diode are provided by the same polycrystalline silicon island; both the p-type and n-type doped regions of the PIN diode are provided by respective of the polycrystalline silicon islands.

Regarding claims 8-9, Takayama, (see figures 9A-9C), teaches a second thin film transistor having doped source/drain regions provided by one of the polycrystalline silicon islands, the doped source/drain regions being of an opposite conductivity type; wherein a transparent conductive gate 19a overlies the intrinsic amorphous silicon region of the PIN diode separated by an insulating layer 15, the gate serving to apply a voltage to the amorphous silicon intrinsic region so as to control the conductivity between the n-type and p-type doped regions.

Regarding claims 10-11, Takayama, (see figures 9A-9C), teaches the thin film transistor further comprises a gate electrode, which serves to control a current through the channel, and wherein the amorphous silicon intrinsic region of the PIN diode overlies the gate electrode; the PIN diode serves to measure a light intensity output from an associated display element and supply a signal to drive circuitry connected to enable modulation of the light intensity output.

### Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Zhang'000 is cited as of interest.
8. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).
9. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792.

The examiner can normally be reached on Monday-Friday from 7:00 AM to 5:30 PM. *The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.*

*Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).*

David Nhu 

August 12, 2007

